

NETL.001DV2



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Jayesh R. Bhakta et al.

Appl. No. : 10/674,082

Filed : September 29, 2003

For : ARRANGEMENT OF INTEGRATED  
CIRCUITS IN A MEMORY MODULE

Examiner : Unknown

Group Art Unit 2818

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Office of Initial Patent Examination, Customer Service Center, Alexandria, VA 22313-1450, on

4/22/04

(Date)  
  
Bruce S. Itchkawitz, Reg. No. 47,677

REQUEST FOR CORRECTED FILING RECEIPT

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Dear Sir:

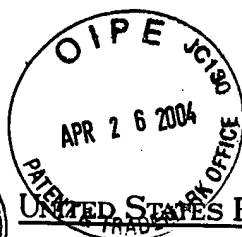
Applicants hereby request that the Official Filing Receipt, a copy of which is enclosed, be corrected to reflect the true filing date of September 29, 2003. Presently, the Filing Receipt incorrectly shows the filing date as September 26, 2003.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 4/22/04

By:   
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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/674,082	09/26/2003 09/29/2003	2818	750	NETL.001DV2	9	18	2

20995  
 KNOBBE MARTENS OLSON & BEAR LLP  
 2040 MAIN STREET  
 FOURTEENTH FLOOR  
 IRVINE, CA 92614

CONFIRMATION NO. 2166

## FILING RECEIPT



\*OC000000012286118\*

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Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

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 Robert S. Pauley JR., San Juan Capistrano, CA;

## Domestic Priority data as claimed by applicant

This application is a DIV of 10/094,512 03/07/2002

## Foreign Applications

If Required, Foreign Filing License Granted: 04/05/2004

Projected Publication Date: 07/15/2004

Non-Publication Request: No

Early Publication Request: No

## Title

Arrangement of integrated circuits in a memory module

## Preliminary Class

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